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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

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EXAMINER
RICHARDS, N DREW

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/605,293	Applicant(s) CHAPEK, DAVID L.	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on Amendment B filed 12/31/01

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 9,10,11,12,14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-12,14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☑ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art.

Applicant's admitted prior art discloses on page 1 lines 12-16 a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon formed on the silicon dioxide, the polycrystalline silicon having a smooth morphology. The admitted prior art discloses the layer of silicon dioxide having been doped with hydrogen ions. The semiconductor substrate is considered as a bottom portion of the silicon dioxide layer with the remaining silicon dioxide layer as the silicon dioxide layer upon the substrate. The admitted prior art of lines 16-22 does not teach the layer of silicon dioxide being free of metal contaminants as the Kaufman ion source causes metal contaminants in the layer.

Applicant's admitted prior art on page 1 line 23 through page 2 line 21 teaches the use of plasma source ion implantation. It teaches the PSII to dope various materials without using a metal grid. It would have been obvious to one or ordinary skill in the art

at the time of the invention to use plasma source ion implantation to implant the hydrogen ions. The motivation for doing so is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities.

3. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art.

Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, silicon dioxide layer, a layer of polycrystalline silicon over the silicon dioxide layer forming a gate, a source and a drain in the substrate. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or being free of metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16. Applicant's admitted prior art also teaches using plasma source ion implantation on page 1 line 23 through page 2 line 21 to implant the hydrogen ions which results is the silicon dioxide being free of metal contaminants.

Burns et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Further, at the time of the invention it would have

been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by plasma source ion implantation. The motivation for doing so is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art to obtain the invention of claims 9.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate source and drain formed on the substrate.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a

gate electrode 504 formed on the insulating layer. Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate being free of metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Applicant's admitted prior art also teaches using plasma source ion implantation on page 1 line 23 through page 2 line 21 to implant the hydrogen ions which results is the silicon dioxide (glass) being free of metal contaminants.

Murata et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Further, at the time of the invention it would have been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by plasma source ion implantation. The motivation for doing so is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art to obtain the invention of claim 14.

Response to Arguments

5. Applicant's arguments filed 12/31/02 have been fully considered but they are not persuasive. Applicant argues that the prior art does not teach a silicon dioxide layer free of metal contaminants. This argument is not persuasive as the admitted prior art teaches the use of PSII to implant which results in the silicon dioxide layer being free of metal contaminants.

6. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation is provided in the admitted prior art. The admitted prior art teaches smaller components for achieving high device packing density and employing thinner and smoother films to achieve the smaller components. The prior art then teaches treating silicon dioxide with hydrogen ions to prepare the surface of the silicon dioxide film for the deposition of a layer of polycrystalline silicon to achieve a thinner and smoother polysilicon film. The prior art then teaches using the Kaufman ion source for the implantation and teaches that the Kaufman resulted in sputtering metal into the silicon dioxide and that the metal contaminates cause damage which increases as the device size decreases. Then the prior art taught PSII as a useful method of ion implantation and described the PSII to

have a conductive chamber that did not have a metal grid, thus no contamination. This is taught on page 1 line 5 through page 2 line 25 of the present application. Therefore, motivation is provided for combining the references and the motivation comes from the reference itself and is proper.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
February 4, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800